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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,673	08/05/2003	Ilia Ovsiannikov	M4065.0734/P734	6886
45374	7590	06/06/2007	EXAMINER	
DICKSTEIN SHAPIRO LLP 1825 EYE STREET, NW WASHINGTON, DC 20006			GILES, NICHOLAS G	
		ART UNIT	PAPER NUMBER	
		2622		
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)
	10/633,673	OVTIANNIKOV ET AL.
	Examiner	Art Unit
	Nicholas G. Giles	2622

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 04/06/2007.
- 2a) This action is FINAL. 2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-70 is/are pending in the application.
- 4a) Of the above claim(s) 18-51 and 56-66 is/are withdrawn from consideration.
- 5) Claim(s) _____ is/are allowed.
- 6) Claim(s) 1-17, 52-55 and 67-70 is/are rejected.
- 7) Claim(s) _____ is/are objected to.
- 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 05 August 2003 is/are: a) accepted or b) objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) All b) Some * c) None of:
1. Certified copies of the priority documents have been received.
2. Certified copies of the priority documents have been received in Application No. _____.
3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) Notice of Informal Patent Application
- 6) Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to claims 1-17, 52-55, and 67-70 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claim 1 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support in the specification for the third or fourth voltage sources claimed. However there is support for interpreting the third and fourth voltage sources actually being control lines and therefore will be treated such in the claim.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1-4, 6-16, 52-55, and 67-70 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kole (U.S. Patent No. 6,501,064) in view of Kokubun et al. (U.S. Pub. No. 2003/0146993) in further view of Merrill (U.S. Pub. No. 2002-0036700).

Regarding claim 1, Kole discloses:

An image array pixel comprising: a charge sharing node; and a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node (7:15-8:10, high and low).

Kole is silent with regards to a first and second voltage sources providing the first and second voltages. Kokubun et al. discloses this in ¶0047, ¶0053-65, and Figs. 3 & 4. An advantage to providing a first and second voltage sources providing the first and second voltages is that voltage sources can be used to provide a desired signal on the signal line used such as Kokubun shows in Fig. 3. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole include first and second voltage sources providing the first and second voltages.

Kole and Kokubun et al. are silent with regards to a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines. Merrill discloses this in ¶0043-0045 and Fig. 7. Note that the row select transistor is after the amplifier and thus would be switchably connected to the high and low levels of select input 71. An advantage to using a row transistor is that rows of pixels can be selectively read out. An Advantage

to having separate control lines for the reset transistor and row select transistor is that pixels can be selectively reset and rows can be selectively read out. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole include a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines.

Regarding claim 2, see the rejection of claim 1 and note that Kole further discloses:

First voltage is higher than said second voltage (7:15-8:10, high and low).

Regarding claim 3, see the rejection of claim 1 and note that Kole discloses a low signal level during integration as a second voltage. Kole is silent with regards to the second voltage being ground potential. Kokubun et al. discloses this in ¶0055 and Fig. 4 where M22 can be seen connected to ground, which is a low signal level. An advantage to doing so is that ground potential is further away from a transistor "turn on" voltage than an arbitrary low signal level voltage thus avoiding a partial transistor "turn on". For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole's low signal level be ground potential.

Regarding claim 4, see the rejection of claim 1 and note that Kole further discloses:

One of said source/drain regions is coupled to only one of said first and second voltages at a time (7:15-8:10 high and low).

Regarding claim 6, see the rejection of claim 1 and note that Kole further discloses:

Pixel is a three-transistor pixel (7:15-8:10).

Regarding claim 7, see the rejection of claim 1 and note that Kole further discloses:

Pixel is a four-transistor pixel (8:11-20).

Regarding claim 8, Kole discloses:

A pixel circuit, comprising: a photo sensor; a storage node for receiving charges from said photo sensor; and a reset transistor for resetting said storage node, said reset transistor being switchably coupled to a first and second voltage level (7:15-8:10, high and low).

Kole and Kokubun et al. are silent with regards to a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines. Merrill discloses this in ¶0043-0045 and Fig. 7. Note that the row select transistor is after the amplifier and thus would be switchably connected to the high and low levels of select input 71. An advantage to using a row transistor is that rows of pixels can be selectively read out. An Advantage to having separate control lines for the reset transistor and row select transistor is that pixels can be selectively reset and rows can be selectively read out. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole include a row select transistor being switchably connected to the first

and second voltages and the reset transistor and row select transistor having their own separate control lines.

Regarding claim 9, see the rejection of claim 8 and note that Kole further discloses:

First voltage level is lower than said second voltage level (7:15-8:10).

Regarding claim 10, see the rejection of claim 1 and note that Kole discloses a low signal level during integration as a second voltage. Kole is silent with regards to the second voltage being ground potential. Kokubun et al. discloses this in ¶0055 and Fig. 4 where M22 can be seen connected to ground, which is a low signal level. An advantage to doing so is that ground potential is further away from a transistor "turn on" voltage than an arbitrary low signal level voltage thus avoiding a partial transistor "turn on". For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole's low signal level be ground potential.

Regarding claim 11, see the rejection of claim 8 and note that Kole further discloses:

Pixel is a three-transistor pixel (7:15-8:10).

Regarding claim 12, see the rejection of claim 8 and note that Kole further discloses:

Pixel is a four-transistor pixel (8:11-20).

Regarding claim 13, Kole discloses:

An image array pixel comprising: a change storing node; a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node; and a source-follower transistor having source/drain regions on opposite sides of a gate of said source-follower transistor, one of said source/drain regions of said source-follower transistor being coupled to said first and second voltage and to said one of said source/drain regions of said reset transistor (7:15-8:10, high and low).

Kole and Kokubun et al. are silent with regards to a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines. Merrill discloses this in ¶0043-0045 and Fig. 7. Note that the row select transistor is after the amplifier and thus would be switchably connected to the high and low levels of select input 71. An advantage to using a row transistor is that rows of pixels can be selectively read out. An Advantage to having separate control lines for the reset transistor and row select transistor is that pixels can be selectively reset and rows can be selectively read out. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole include a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines.

Regarding claim 14, see the rejection of claim 13 and note that Kole further discloses:

First voltage is higher than said second voltage (7:15-8:10).

Regarding claim 15, see the rejection of claim 1 and note that Kole discloses a low signal level during integration as a second voltage. Kole is silent with regards to the second voltage being ground potential. Kokubun et al. discloses this in ¶0055 and Fig. 4 where M22 can be seen connected to ground, which is a low signal level. An advantage to doing so is that ground potential is further away from a transistor “turn on” voltage than an arbitrary low signal level voltage thus avoiding a partial transistor “turn on”. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole’s low signal level be ground potential.

Regarding claim 16, see the rejection of claim 13 and note that Kole further discloses:

First source/drain of reset transistor is coupled only to one of said first and second voltages at a time (7:15-8:10).

Regarding claim 52, Kole discloses:

A processing system, comprising: a processor (inherent); an imager array coupled to said processor, one pixel of said image array comprising: a charge sharing node; and a reset transistor having source/drain regions on opposite sides of a gate of said reset transistor, one of said source/drain regions being switchably coupled to a first and second

voltage, the other of said source/drain regions being coupled to said node (7:15-8:10, high and low).

Kole and Kokubun et al. are silent with regards to a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines. Merrill discloses this in ¶0043-0045 and Fig. 7. Note that the row select transistor is after the amplifier and thus would be switchably connected to the high and low levels of select input 71. An advantage to using a row transistor is that rows of pixels can be selectively read out. An Advantage to having separate control lines for the reset transistor and row select transistor is that pixels can be selectively reset and rows can be selectively read out. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole include a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines.

Regarding claim 53, see the rejection of claim 52 and note that Kole further discloses:

First voltage is higher than said second voltage (7:15-8:10).

Regarding claim 54, see the rejection of claim 1 and note that Kole discloses a low signal level during integration as a second voltage. Kole is silent with regards to the second voltage being ground potential. Kokubun et al. discloses this in ¶0055 and Fig. 4 where M22 can be seen connected to ground, which is a low signal level. An advantage to doing so is that ground potential is further away from a transistor "turn on"

voltage than an arbitrary low signal level voltage thus avoiding a partial transistor "turn on". For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole's low signal level be ground potential.

Regarding claim 55, see the rejection of claim 52 and note that Kole further discloses:

One of said source/drain regions is coupled to only one of said first and second voltages at a time (7:15-8:10).

Regarding claim 67, Kole discloses:

An imaging device, comprising: a processor (inherent); an imager array coupled to said processor, one pixel of said image array comprising: a charge sharing node; and a reset transistor having source/drain regions on opposite sides of a gate, one of said source/drain regions being switchably coupled to a first and second voltage, the other of said source/drain regions being coupled to said node (7:15-8:10, high and low).

Kole and Kokubun et al. are silent with regards to a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines. Merrill discloses this in ¶0043-0045 and Fig. 7. Note that the row select transistor is after the amplifier and thus would be switchably connected to the high and low levels of select input 71. An advantage to using a row transistor is that rows of pixels can be selectively read out. An Advantage to having separate control lines for the reset transistor and row select transistor is that pixels can be selectively reset and rows can be selectively read out. For this reason it

would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole include a row select transistor being switchably connected to the first and second voltages and the reset transistor and row select transistor having their own separate control lines.

Regarding claim 68, see the rejection of claim 67 and note that Kole further discloses:

First voltage is higher than said second voltage (7:15-8:10).

Regarding claim 69, see the rejection of claim 1 and note that Kole discloses a low signal level during integration as a second voltage. Kole is silent with regards to the second voltage being ground potential. Kokubun et al. discloses this in ¶0055 and Fig. 4 where M22 can be seen connected to ground, which is a low signal level. An advantage to doing so is that ground potential is further away from a transistor “turn on” voltage than an arbitrary low signal level voltage thus avoiding a partial transistor “turn on”. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole’s low signal level be ground potential.

Regarding claim 70, see the rejection of claim 67 and note that Kole further discloses:

One of said source/drain regions is coupled to only one of said first and second voltages at a time (7:15-8:10).

6. Claims **5 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Kole in view of Kokubun et al. in further view of Merrill in further view of Mizuno et al. (U.S. Patent No. 5,912,463).

Regarding claim **5**, see the rejection of claim 1 and note that Kole is silent with regards to the pixel not receiving any light. Mizuno et al. discloses this in 8:52-59. An advantage to doing so is that dark current can be read out for image correction. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole's pixels not receive any light.

Regarding claim **17**, see the rejection of claim 1 and note that Kole is silent with regards to the pixel not receiving any light. Mizuno et al. discloses this in 8:52-59. An advantage to doing so is that dark current can be read out for image correction. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Kole's pixels not receive any light.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

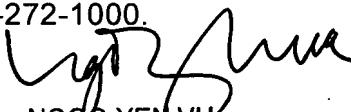
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas G. Giles whose telephone number is (571) 272-2824. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ngoc - Yen Vu can be reached on (571) 272-7320. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


NGOC-YEN VU
SUPERVISORY PATENT EXAMINER